Attorney Docket No.: 5649-1098 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Moon et al.
Serial No.: 10/715,015
Filed: November 17, 2003
For: VARIABLE-DELAY PRECHARGE CIRCUITS AND METHODS

Group Art Unit: 2824
Examiner: Jung H. Hur
Confirmation No.: 3312

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APPELLANTS' BRIEF ON APPEAL UNDER 37 C.F.R. §41.37

Sir:

This Appeal Brief is filed pursuant to the "Notice of Appeal to the Board of Patent Appeals and Interferences" filed April 7, 2006.

It is not believed that an extension of time and/or additional fee(s) are required, beyond those that may otherwise be provided for in documents accompanying this paper. In the event, however, that an extension of time is necessary to allow consideration of this paper, such an extension is hereby petitioned under 37 C.F.R. Sec. 1.136(a). Any additional fees believed to be due may be charged to Deposit Account No. 50-0220.

Real Party In Interest

The real party in interest is assignee Samsung Electronics Co. Ltd., Republic of Korea.

Related Appeals and Interferences

Appellants are aware of no appeals or interferences that would be affected by the present appeal.

Status of Claims

In a Final Office Action mailed December 7, 2005 (hereinafter "Final Action"), Claims 1, 4-10, 15 and 16 as presented in Appellants' Amendment filed September 21, 2005 (hereinafter "First Amendment") were rejected. The Final Action indicated that Claims 11-14

would be allowable if rewritten in independent form including recitations from base and intervening claims. In response to the Final Action, Appellants submitted an Amendment After Final Action on January 25, 2006 (hereinafter "Amendment After Final"). An Advisory Action mailed February 15, 2006 indicated that the amendments in the Amendment After Final would be entered for purposes of appeal. Appellants appeal the final rejections of Claims 1, 4-10, 15 and 16 as presented in the Amendment After Final.

Status of Amendments

Appellants' Amendments of April 4, 2005 and September 21, 2005 have been entered. Responsive to the Final Action, the Amendment After Final amended Claim 1. The attached Appendix A presents the pending Claims 1 and 4-16 as amended in the Amendment After Final, which has been entered with the filing of this Appeal. The claims presented in Appendix A are currently pending for consideration in this Appeal.

Summary of Claimed Subject Matter

According to independent Claim 1, a memory device includes a data line (see e.g., FIG. 2, reference IO, IOB) and a variable delay precharge circuit (*see, e.g.*, FIG. 2, reference 2000) that receives a column bank address signal and a write enable signal and that precharges the data line responsive to the column bank address signal at a time that is determined by a state of the write enable signal. The variable delay precharge circuit includes a precharge circuit (*see, e.g.*, FIG. 2, reference 250) operative to precharge the data line responsive to a precharge control signal. The variable delay precharge circuit also includes a precharge control signal generator circuit (*see, e.g.*, FIG. 2, reference 200) that receives the column bank address signal, that generates first and second delayed signals from the column bank address signal that are delayed by respective different first and second time periods with respect to the column bank address signal, and that applies to the precharge circuit, responsive to a precharge delay control signal, a selected one of a first precharge control signal generated from the first delayed signal and a second precharge control signal generated from the second delayed signal. The variable delay precharge circuit further includes a precharge delay control circuit (*see, e.g.*, FIG. 2, reference 210) that generates the precharge delay control signal responsive to the write enable signal.

According to independent Claim 6, a memory device includes a pair of data input/output lines and a precharge circuit that precharges the pair of data input/output lines

responsive to a precharge control signal. The memory device also includes a precharge control signal generator circuit that receives a column bank address signal, that generates first and second delayed signals from the column address bank signal that are delayed by respective different first and second time periods with respect to the column address bank signal, and that applies to the precharge circuit, responsive to a precharge delay control signal, a selected one of a first precharge control signal generated from the first delayed signal and a second precharge signal generated from the second delayed signal. The memory device further includes a precharge delay control circuit that generates the precharge delay control signal responsive to a write enable signal.

According to independent Claim 9, a precharge control circuit for controlling a precharge circuit of a semiconductor memory device includes a precharge control signal generator circuit that receives a column bank address signal, that generates first and second delayed signals from the column address bank signal that are delayed by respective different first and second time periods, and that applies, responsive to a precharge delay control signal, a selected one of a first precharge control signal generated from the first delayed signal and a second precharge control signal generated from the second delayed signal. The precharge control circuit further includes a precharge delay control circuit that generates the precharge delay control signal responsive to a write enable signal. The precharge delay control circuit causes application of the first precharge control signal after a read operation of the memory device and application of the second precharge control signal after a write operation of the memory device.

According to independent Claim 15, methods of generating a precharge control signal for a precharge circuit of a memory device include receiving a column bank address signal, generating a first delayed signal and a second delayed signal from the column bank address signal that are delayed respective first and second time periods, and selectively generating the precharge control signal from one of the first delayed signal or the second delayed signal based on a state of a write enable signal. The first time period is greater than the second time period.

Grounds of Rejection To Be Reviewed on Appeal

Independent Claims 1, 6, 9 and 15 stand rejected under 35 U.S.C. §103(a) as unpatentable over a combination of alleged admitted prior art (hereinafter "Admission") and U.S. Patent No. 5,828,612 to Yu et al. (hereinafter "Yu"). In the following remarks, the

Appellants will show that independent Claims 1, 6, 9 and 15 are patentable over this combination. Appellants will further show that dependent Claims 4, 5, 7, 8, 10-14 and 16 are patentable at least by virtue of the patentability of the respective ones of independent Claims 1, 6, 9 and 15 from which they depend. As acknowledged in the Final Action, Claims 11-14 are also separately patentable.

Arguments

I. Introduction

The pending claims are rejected as obvious under 35 U.S.C. § 103. To establish a prima facie case of obviousness, the prior art reference or references when combined must teach or suggest *all* the recitations of the claims, and there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. M.P.E.P. §2143. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. M.P.E.P. §2143.01, citing *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990). As emphasized by the Court of Appeals for the Federal Circuit, to support combining references, evidence of a suggestion, teaching, or motivation to combine must be clear and particular, and this requirement for clear and particular evidence is not met by broad and conclusory statements about the teachings of references. *In re Dembiczak*, 50 U.S.P.Q.2d 1614, 1617 (Fed. Cir. 1999). The Court of Appeals for the Federal Circuit has further stated that, to support combining or modifying references, there must be particular evidence from the prior art as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed. *In re Kotzab*, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000).

Appellants respectfully submit that the rejections of Claims 1, 4-10, 15 and 16 are erroneous because the cited combination of references fails to disclose or suggest all of the recitations of the pending claims, and because the Final Action fails to provide the requisite clear and particular evidence from the prior art of a motivation or suggestion to combine the references as proposed in the Final Action. Appellants, therefore, request reversal of the rejections.

II. Independent Claims 1, 6, 9 and 15 Are Patentable

Claim 1 recites, in part:

> . . . a precharge control signal generator circuit that receives the column bank address signal, that generates first and second delayed signals from the column address bank signal that are delayed by respective different first and second time periods with respect to the column bank address signal, and that applies to the precharge circuit, responsive to a precharge delay control signal, a selected one of a first precharge control signal generated from the first delayed signal and a second precharge control signal generated from the second delayed signal; and
>
> a precharge delay control circuit that generates the precharge delay control signal responsive to the write enable signal.

The description of FIGs. 1A and 1B in the Background of the Invention section of the present application, *i.e.*, Admission, clearly does not disclose or suggest a memory device in which a precharge control signal generator circuit "generates first and second delayed signals from the column address bank signal that are delayed by respective different first and second time periods with respect to the column bank address signal" and "a first precharge control signal generated from the first delayed signal and a second precharge control signal generated from the second delayed signal." Rather, FIGs. 1A and 1B describe a circuit that generates a precharge control signal responsive only to a column bank address signal CBA.

Yu fails to provide the missing teachings. Yu describes providing different precharge timings for write and read cycles, but Yu describes generating these different precharge timings in a manner that is distinctly different from that recited in the claims and, therefore, Yu does not provide the teachings alleged in the Final Action. In particular, Yu does not generate "first and second delayed signals from the column address bank signal that are delayed by respective different first and second time periods with respect to the column bank address signal" and does not apply "to the precharge circuit, responsive to a precharge delay control signal, a selected one of a first precharge control signal generated from the first delayed signal and a second precharge control signal generated from the second delayed signal." Rather, Yu generates only a DEFAULT PRECHARGE TRIGGER (see Yu, FIGs. 2 and 4) responsive to an address signal A_X; there is nothing in Yu corresponding to the recited "first and second delayed signals" or the recited "first precharge control signal generated from the first delayed signal and a second precharge control signal generated from the second delayed signal." Accordingly, even if combined, Admission and Yu do not disclose or suggest all of the recitations of independent Claim 1.

Appellants further submit that the Final Action provides insufficient evidence of a motivation or suggestion to combine Admission and Yu. As noted above, Yu describes a technique for providing different precharge timings for read and write cycles, but this is not clear and particular evidence of a teaching or suggestion to modify the device described in the Background of the Invention ***in the specific manner recited in Claim 1***, as neither Yu nor the Background of the Invention disclose or suggest this specific approach.

The reasoning provided on pages 4 and 7 of the Final Action as a basis for modifying the device described in the Background is erroneous. In particular, the Final Action states:

> . . . it would have been obvious to . . . modify the device and the relate method of Admission to generate a second precharge control signal responsive to the bank address signal . . ., and to select the first precharge control signal for a read operation and the second precharge control signal for a write operation, determined by the write enable signal (for example, using a multiplexer, commonly used and well known in the art), for the purpose of increasing the frequency of operation.

(Final Action, p. 4). This reasoning relies on a series of inferences that are not supported by the prior art in evidence. In particular, as noted above, Yu already proposes a different way of generating different read and write cycle precharge timings, one that does not involve the operations described in the above-quoted passage from page 4 of the Final Action. The Final Action provides no evidence from the prior art as to how or why applying this approach to the circuitry described in the Background of the Invention would result in the recitations of Claim 1. Moreover, references to addition of a "multiplexer" and other modifications of the circuitry described in the Background of the Invention are simply hindsight reconstruction, unsupported by any particular evidence from the prior art. Accordingly, Appellants submit that the Final Action fails to provide the requisite evidence of a suggestion or motivation to combine Admission and Yu in the manner proposed in the Final Action.

In light of the foregoing, Appellants submit that the rejection of independent Claim 1 is erroneous and should be reversed. At least similar reasons support reversal of the rejections of independent Claims 6, 9 and 15. For example, for at least reasons similar to those discussed above, the combination of Admission and Yu does not disclose or suggest:

> . . . a precharge control signal generator circuit that receives a column bank address signal, that generates ***first and second delayed signals*** from the column address bank signal that are delayed by respective different first and second time periods with respect to the column address bank signal, and that applies to the precharge circuit, responsive to a precharge delay control signal, a selected one of ***a***

> ***first precharge control signal generated from the first delayed signal and a second precharge signal generated from the second delayed signal*** . . .

as recited in independent Claim 6. Similarly, Admission and Yu do not disclose or suggest:

> . . . a precharge control signal generator circuit that receives a column bank address signal, that generates ***first and second delayed signals*** from the column address bank signal that are delayed by respective different first and second time periods, and that applies, responsive to a precharge delay control signal, a selected one of ***a first precharge control signal generated from the first delayed signal and a second precharge control signal generated from the second delayed signal*** . . .

as recited in independent Claim 9, or

> . . . generating ***a first delayed signal and a second delayed signal*** from the column bank address signal that are delayed respective first and second time periods;
> ***selectively generating the precharge control signal from one of the first delayed signal or the second delayed signal based on a state of a write enable signal.***

as recited in independent Claim 15.

III. Dependent Claims 4, 5, 7, 8, 10-14 and 16 Are Patentable

Appellants submit that dependent Claims 4, 5, 7, 8, 10-14 are patentable at least by virtue of the patentability of the respective ones of independent Claims 1, 6, 9 and 15 from which they depend. Appellants further note the Final Action confirms that Claims 11-14 are separately patentable.

IV. Conclusion

For at least the reasons discussed above, Appellants, therefore, request reversal of the rejections of Claims 1, 4-10, 15 and 16.

Respectfully submitted,

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Appendix A: Claims

1. (Rejected) A memory device, comprising:

a data line; and

a variable delay precharge circuit that receives a column bank address signal and a write enable signal and that precharges the data line responsive to the column bank address signal at a time that is determined by a state of the write enable signal, wherein the variable delay precharge circuit comprises:

a precharge circuit operative to precharge the data line responsive to a precharge control signal;

a precharge control signal generator circuit that receives the column bank address signal, that generates first and second delayed signals from the column bank address signal that are delayed by respective different first and second time periods with respect to the column bank address signal, and that applies to the precharge circuit, responsive to a precharge delay control signal, a selected one of a first precharge control signal generated from the first delayed signal and a second precharge control signal generated from the second delayed signal; and

a precharge delay control circuit that generates the precharge delay control signal responsive to the write enable signal.

2-3. (Canceled)

4. (Rejected) The memory device of Claim 1, wherein the variable delay precharge circuit precharges the data line after a first predetermined time period following assertion of the column bank address signal when the write enable signal indicates a read operation, and wherein the variable delay precharge circuit precharges the data line after a second predetermined time period following assertion of the column bank address signal when the write enable signal indicates a write operation.

5. (Rejected) The memory device of Claim 4, wherein the second time period is shorter than the first time period.

6. (Rejected) A memory device comprising:

a pair of data input/output lines;

a precharge circuit that precharges the pair of data input/output lines responsive to a precharge control signal;

a precharge control signal generator circuit that receives a column bank address signal, that generates first and second delayed signals from the column address bank signal that are delayed by respective different first and second time periods with respect to the column address bank signal, and that applies to the precharge circuit, responsive to a precharge delay control signal, a selected one of a first precharge control signal generated from the first delayed signal and a second precharge signal generated from the second delayed signal; and

a precharge delay control circuit that generates the precharge delay control signal responsive to a write enable signal.

7. (Rejected) The memory device of claim 6, wherein the first precharge control signal rises in synchronization with a rising edge of the column bank address signal and falls the first period of time after an immediately succeeding falling edge of the column bank address signal, and wherein the second precharge control signal rises in synchronization with a rising edge of the column bank address signal and falls the second period of time after an immediately succeeding falling edge of the column bank address signal.

8. (Rejected) The memory device of claim 6, wherein the pair of data input/output lines are a pair of global input/output lines of the memory device.

9. (Rejected) A precharge control circuit for controlling a precharge circuit of a semiconductor memory device, the precharge control circuit comprising:

a precharge control signal generator circuit that receives a column bank address signal, that generates first and second delayed signals from the column address bank signal that are delayed by respective different first and second time periods, and that applies, responsive to a precharge delay control signal, a selected one of a first precharge control signal generated from the first delayed signal and a second precharge control signal generated from the second delayed signal; and

a precharge delay control circuit that generates the precharge delay control signal responsive to a write enable signal,

wherein the precharge delay control circuit causes application of the first precharge control signal after a read operation of the memory device and application of the second precharge control signal after a write operation of the memory device.

10. (Rejected) The precharge control circuit of claim 9, wherein the first period of time is longer than the second period of time.

11. (Objected to) The precharge control circuit of claim 9, wherein the control circuit comprises:

a first delay that receives the write enable signal and outputs an inverted delayed signal therefrom;

a NAND circuit that receives the write enable signal and the inverted delayed signal output from the first delay, performs a NAND operation on the write enable signal and the inverted signal, and responsively outputs a signal; and

a latching/inverting circuit that receives, latches, and inverts the signal output from the NAND circuit and the first delay signal, and responsively outputs a signal.

12. (Objected to) The precharge control circuit of claim 11, wherein the first delay comprises an odd number of inverters connected in series.

13. (Objected to) The precharge control circuit of claim 11, wherein the precharge control signal generator circuit comprises:

a first NOR circuit that receives the second delayed signal and the signal output from the latching/inverting circuit, performs a NOR operation on the second delayed signal and the signal output from the latching/inverting circuit, and responsively outputs a first signal;

a second NOR circuit that receives the column bank address signal and the first delayed signal, performs a NOR operation for the column bank address signal and the first delayed signal, and responsively outputs a second signal; and

a third NOR circuit that receives the first and second signals output from the first and second NOR circuits, performs a NOR operation on the first and second signals, and responsively outputs a third signal.

14. (Objected to) The precharge control circuit of claim 13, wherein, if the write enable signal indicates a write operation, the precharge control signal generator circuit generates the first precharge control signal, and wherein, if the write enable signal indicates a read operation, the precharge control signal generator circuit generates the second precharge signal.

15. (Rejected) A method of generating a precharge control signal for a precharge circuit of a memory device, the method comprising:

receiving a column bank address signal;

generating a first delayed signal and a second delayed signal from the column bank address signal that are delayed respective first and second time periods;

selectively generating the precharge control signal from one of the first delayed signal or the second delayed signal based on a state of a write enable signal,

wherein the first time period is greater than the second time period.

16. (Rejected) The method of claim 15, wherein the precharge control signal is generated from the first delayed signal responsive to a read operation of the memory device, and wherein the second precharge control signal is generated from the second delayed signal responsive to a write operation of the memory device.

Appendix B: Evidence

No evidence pursuant to 37 C.F.R. Sec. 1.130, Sec. 1.131, or Sec. 1.132 is relied upon by Appellants in this Appeal.

Appendix C: Related Proceedings

There are no related proceedings pursuant to 37 C.F.R. Sec. 41.37.